# Thales Communications SDR and JTRS

## **Products**

### **Software Defined Radios**



#### **MSHR**

- Type 1 & 3
- Voice & Data



#### AN/PRQ-7 (CSEL)

- Global Satellite Comms
- Voice & Data
- LPI/D Waveform



#### LW Squad Radio

- Type 1 Voice & Data
- SINCGARS SIP



#### Thales 25

- APCO Project 25
- Narrowband Digital
- DES Voice & Data



- Type 1 Voice & Data
- SINCGARS SIP
- HAVEQUICK II
- ANDVT

## JTRS Cluster 2 Step 2B



Independent Validation of SCA

Thousands of software-based radio products sold





# **SCA Objectives - Signal Processing**

## Subsystem

## Reconfigurability

- Platform scaleable
- Partial downloading

## **Portability**

- HW abstraction
- Standard APIs

## **Ease of Development**

- Coding standards
- Standard architecture
- Common services and libraries





## **Signal Processing Subsystem Constraints**

# SCA and Portability impose overhead on Real-time Signal Processing Subsystems

- CORBA
- Object-oriented development environment for fixed point DSPs
- Memory constraints
- FPGA constraints

### Historic SPS design different than control software

- Signal modeling versus object modeling
- Signal simulation versus process simulation

## Historic SPS implementation paradigm different than control software

- Data flow-oriented versus object-oriented
- Serial processes versus multiple threads
- Performance optimization typically stressed over portability





## A Potential DSP Approach: HAL Architecture

#### **Platform Services**

**DSP Framework RTOS** 

- Abstraction of DSP RTOS semantics
- ■POSIX-oriented profile

**DSP Manager** 

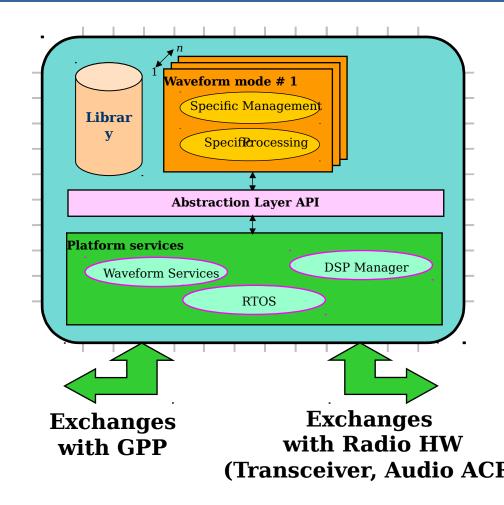
- ■DSP SW Configuration / Deployment
- Similar to SCA Resource interface

Interface Services - Rx/Tx Interfaces

- ■API for Rx/Tx exchanges with GPP
  - Modem GPP Services Interface
  - Audio\_GPP Services Interface
- ■API for Rx/Tx exchanges with Radio HW
  - Modem\_Transceiver Services Interface
  - Audio Audio Services Interface

#### Libraries

- ■CVSD Voice Coder
- ■FFT, Viterbi,...



Performance Driven DSP Framework C Language, RTOS, Signal Processing Library, open APIs, ...





## **FPGA Considerations**



#### **Standardized Internal Architecture**

- Virtual Socket Interface Alliance (VSIA)
- Altera Avalon<sup>™</sup> switch fabric
- Parameterized Library of Signal Processing Functions

#### Standard External Interfaces

- Status Registers for configuration information, version, etc.
- High Speed and Low Speed standard interfaces
- Efficient Data Exchange / DMA standards

#### **Development Guidelines**

- Coding Standards IEEE 1076 VHDL and IEEE 1364 Verilog
- Design standards to focus on portability, but still allow for optimization in implementation environment
- OpenMORE IP reuse assessment
- Automated code generation from simulation and modeling tools

#### **Dynamic Reconfigurability**

- Instantiation of waveforms in real-time
- Partial reconfiguration

